## REMARKS

Applicants thank the Examiner for the thorough examination of the application.

Claims 1, 3-10, 12, 13, 15-18 and 21-25 are pending in this application. Claims 1, 10 and 25 are independent.

Claims 1, 3, 4, 8-10, 12, 13, 17 and 18 are amended. Claims 2, 11, 14, 19 and 20 are canceled without prejudice to or disclaimer of the subject matter contained therein. Claims 21-25 are added.

Reconsideration of the present application, as amended, is respectfully requested.

### ***Drawings***

Applicants have not received a Notice of Draftsperson's Patent Drawing Review, Form PTO-948, indicating whether the formal drawings have been approved by the Official Draftsperson. It is respectfully submitted that the drawings comply with USPTO requirements. Clarification with the next official communication is respectfully requested.

***Rejection under 35 U.S.C. §103(a)***

Claims 1-3, 5, 6, 8, 10-12, 14, 15, 17, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,429,909 to Kim et al. in view of U.S. Patent No. 6,313,889 to Song et al. Claims 8 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kim et al. in view of Song et al., and further in view of U.S. Patent No. 5,657,101 to Cheng. Claims 4, 7, 9, 13, 16 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kim et al. in view of Song et al., and further in view of U.S. Patent No. 5,734,450 to Irie et al. These rejections, to the extent that they apply to the presently pending claims, are respectfully traversed.

While not conceding the appropriateness of the rejections, but merely to advance prosecution of the instant application, independent claim 1 is amended to recite a combination of elements in a thin film transistor substrate in a liquid crystal display, including "a gate dummy pattern formed ... to overlap with at least one of edge portions of the data line and an edge portion of the pixel electrode."

Independent claim 10 is amended to recite a combination of elements in a thin film transistor substrate in liquid crystal display, including "a gate dummy pattern formed ... to overlap by about 0.5-1 μm with at least one of the data line and an edge portion of the pixel electrode."

It is respectfully submitted that the combinations of elements set forth in independent claims 1 and 10 are not disclosed or rendered obvious by the applied prior art of record, including Kim et al., Song et al, Cheng or Irie et al.

Kim et al. discloses an LCD including a repair line 120, a gate insulating film 200, a data line 400, a passivation film 500, and a pixel electrode 600 formed sequentially on a transparent insulating substrate 10, as shown in FIG. 7. The Office Action equates the repair line 120 in Kim et al. with the claimed "gate dummy pattern" of the present invention. However, the repair line 120 in Kim et al. is positioned such that the data line 400 is formed only over a central portion of the repair line 120 and the pixel electrode 600 is formed over each side of the repair line 120. By contrast, in the present invention, the data line and the pixel electrode are each formed to overlap with different sides of the gate dummy pattern. Kim et al. does not teach or suggest a "a gate dummy pattern formed to overlap with at least one of edge portions of the data line and an edge portion of the pixel electrode," as recited in claim 1. Likewise, Kim et al. does not teach or suggest "a gate dummy pattern formed to overlap by about 0.5-1 μm with at least one of the data line and an edge portion of the pixel electrode," as recited in claim 10.

The Office Action relies on Song et al. for teachings of the use of a redundant pattern that is integrated with a gate line, a redundancy electrode that electrically connects the gate line to the broken data line, and a storage capacitor defined by a

horizontal overlapping part between the gate line and the pixel electrode. However, Song et al. does not teach or suggest the above-cited limitation of claims 1 and 10 and, therefore, fails to cure the deficiencies of Kim et al. with respect to these claims.

In rejecting claims 8 and 17, the Office Action relies on Cheng for a teaching of patterns made from a gate metal layer on both sides of a data line. Cheng discloses an LCD including a storage electrode 52, a gate insulator layer 43 and a data line 59 formed sequentially on a glass substrate, as shown in FIG. 5d. The storage electrode 52, which the Office Action appears to equate with the claimed "gate dummy pattern," is formed under and adjacent to each side of the data line 59. However, the data line 59 is not formed over any side of the storage electrode 52. Accordingly, Cheng does not teach or suggest the above-cited limitations of claims 1 and 10 and, therefore, fails to cure the deficiencies of Kim et al. and Song et al. with respect to the claims 1 and 10, incorporated in claims 8 and 17.

In rejecting claims 4, 7, 9, 13, 16 and 18, the Office Action relies on Irie et al. for a teaching of a recess in the dummy pattern. However, Irie et al. does not teach or suggest the above-cited limitation of claims 1 and 10 and, therefore, fails to cure the deficiencies of Kim et al. and Song et al. with respect to the claims 1 and 10, incorporated in claims 4, 7, 9, 13, 16 and 18.

In view of the foregoing, it is respectfully submitted that the applied prior art of record, including Kim et al., Song et al., Cheng and Irie et al., fails to teach or

suggest the combinations of elements set forth in independent claims 1 and 10. It is believed that claims 1 and 10 are allowable. Since the remaining claims depend from allowable claims, they are also allowable for at least the above reasons, as well as for the additional limitations provided thereby. Thus, all claims are allowable. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §103(a) are respectfully requested.

***Added Claims***

Claims 21-25 have been added for the Examiner's consideration. Applicants respectfully submit that claims 21-24 depend, either directly or indirectly, from independent claims 1 and 10, and are therefore allowable based on their dependence from claims 1 and 10, which are believed to be allowable.

In addition, claims 21-24 recite further limitations which are not disclosed or made obvious by the applied prior art references.

Independent claim 25 recites a combination of elements in a thin film transistor substrate for a display device including "a gate dummy pattern including first and second extension parts extending from the gate line in the first direction and separated from each other, the first extension part disposed below a first edge portion of the data line and a side portion of an adjacent pixel electrode, the second extension part disposed below a second edge portion of the data line

and a side portion of another adjacent pixel electrode, the first and second edge portions being opposite edge portions of the data line." Applicants respectfully submit that this combination of elements as set forth in independent claim 25 is not disclosed or made obvious by the applied prior art of record.

## CONCLUSION

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

However, if there are any outstanding issues, the Examiner is invited to telephone Sam Bhattacharya (Reg. No. 48,107) at (703) 205-8000 in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or to credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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